



INITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Kao et al.

Docket No:

16405-0311

Serial No:

09/256,265

Group Art Unit

2815

Filing Date:

February 23, 1999

Examiner:

Diaz, J.

Title:

"METHOD AND APPARATUS FOR SPLIT GATE SOURCE SIDE

INJECTION FLASH MEMORY CELL AND ARRAY WITH

DEDICATED ERASE GATES"

Commissioner for Patents Washington, D.C. 20231

Sir:

AMENDMENT

Responsive to the Office Action mailed March 13, 2002, please amend the above-

identified application as follows:

In the Claims:

Please amend the claims as follows:

1. (Amended) A semiconductor device having at least one transistor, the device

comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of

said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said

9 floating gate;

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a control gate having a first/portion disposed over a portion of said channel region and

being separated therefrom by said second insulating layer, a second portion formed over a first

one of said side walls and a third portion formed over at least a portion of said top surface of said 12 %%121/2008 MAGARMI 00000185 013884 39353665

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